

CLAIMS

What is claimed is:

- 1 1. A System-On-Chip (SOC) architecture comprising:
 - 2 a system bus;
 - 3 a processor in communication with the system bus;
 - 4 an input/output (I/O) interface in communication with the system bus; and
 - 5 a ferroelectric memory component in communication with the system bus.

- 1 2. The SOC of claim 1, further comprising debugging and self-test modules in
2 communication with the system bus.

- 1 3. The SOC of claim 1, further comprising a direct memory access (DMA)
2 component in communication with the system bus.

- 1 4. The SOC of claim 1, further comprising a memory controller in
2 communication with the system bus.

- 1 5. The SOC of claim 1, further comprising re-configurable hardware in
2 communication with the system bus.

- 1 6. The SOC of claim 5, wherein the re-configurable hardware has a ferroelectric
2 memory component embedded therein, and wherein the re-configurable hardware has
3 a configuration that is stored in the ferroelectric memory component embedded in the
4 re-configurable hardware.

- 1 7. The SOC of claim 5, wherein the ferroelectric memory component embedded
2 in the re-configurable hardware is a ferroelectric random access memory (FeRAM)
3 component.

- 1 8. The SOC of claim 1, wherein the ferroelectric memory component is a
2 ferroelectric random access memory (FeRAM) component.

- 1 9. The SOC of claim 1, wherein the processor is a microprocessor.

1 10. The SOC of claim 1, wherein the processor is a microcontroller.

1 11. The SOC of claim 1, wherein the ferroelectric memory component stores
2 programs and data needed by the processor for execution of the programs by the
3 processor, and wherein, during execution of a program by the processor, the processor
4 causes an instruction pointer to be stored in a predetermined location in the
5 ferroelectric memory component that identifies a location in the ferroelectric memory
6 component that contains an address of a next instruction to be executed by the
7 processor.

1 12. The SOC of claim 11, wherein the SOC comprises a re-configurable hardware
2 component in communication with the system bus, and wherein the processor causes
3 the configuration of the re-configurable hardware component to be stored in the
4 ferroelectric memory component.

1 13. The SOC of claim 12, wherein when the re-configurable hardware is
2 executing, current state values of the re-configurable hardware are stored at
3 predetermined locations in the ferroelectric memory component, and wherein if a
4 power cycle occurs, then when power returns, the processor uses the instruction
5 pointer to obtain the next instruction to be executed and resumes execution of the
6 program.

1 14. The SOC of claim 13, wherein if a power cycle occurs, when power returns,
2 said current state values are read out of the ferroelectric memory component and used
3 by the re-configurable hardware to resume execution of the re-configurable hardware.

1 15. The SOC of claim 1, further comprising an intellectual property (IP) hardware
2 component in communication with the system bus.

1 16. The SOC of claim 15, further comprising an input/output (I/O) hardware
2 component in communication with the system bus.

1 17. The SOC of claim 16, further comprising a static random access memory
2 component.

1 18. The SOC of claim 17, further comprising a dynamic random access memory
2 (DRAM) component.

1 19. A method for preventing an occurrence of a power cycle in a System-On-Chip
2 (SOC) architecture from requiring that the SOC be rebooted and re-initialized, the
3 method comprising the steps of:

4 storing, in a ferroelectric memory component embedded in the SOC, an
5 address pointer to an address location in the ferroelectric memory component that
6 contains a next instruction to be executed by a processor embedded in the SOC, said
7 next instruction being part of an instruction set currently being executed by the
8 processor;

9 after a power cycle has occurred, when power returns, accessing by the
10 processor said next instruction, the processor using the address pointer to access said
11 next instruction; and

12 executing, in the processor said next instruction, thereby resuming execution
13 of the instruction set.

1 20. The method of claim 19, wherein the ferroelectric memory component is a
2 ferroelectric random access memory (FeRAM) component.

1 21. The method of claim 19, wherein the SOC has re-configurable hardware
2 embedded therein, and wherein the method further comprises the step of:

3 prior to the occurrence of the power cycle, storing a configuration of the re-
4 configurable hardware and current state of the re-configurable hardware in the
5 ferroelectric memory component.

1 22. A computer program for use in a System-On-Chip (SOC) architecture, the
2 computer program being embodied on a computer readable medium, the program
3 comprising:

4 a first code segment for storing, during execution of an instruction set, an
5 address pointer in a ferroelectric memory device, the address pointer pointing to a
6 location in the ferroelectric memory component that contains a next instruction of the
7 instruction set to be executed; and

8 a second code segment for utilizing the address pointer to access the location
9 in the ferroelectric memory component that contains said next instruction, said second
10 segment being executed after a power cycle has occurred.

PAGES 15 OF 15